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Implementation of UART with BIST Technique Using Low Power LFSR

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Abstract
Asynchronous serial communication is usually implemented by Universal Asynchronous Receiver Transmitter (UART), mostly used for low expense, low speed, short distance data exchange between processor and peripherals. UART allows full duplex serial communication link, and is used in data communication and control system. There is a need for realizing the UART function in a single or a very few chips. Further, design systems without full testability are open to the increased possibility of product failures and missed market opportunities. Also, it is necessary to ensure the data transfer is error proof. This project targets the introduction of Built-in self test (BIST) and Status register to UART. The basic idea is to reduce the switching activity among the test patterns at the most. In this approach, the single input change patterns generated by a counter and a gray code generator are Exclusive-ORed with the seed generated by the low power linear feedback shift register [LP-LFSR]. The 8-bit UART with status register and BIST module is coded in Verilog HDL and synthesized and simulated using Xilinx XST and ISim version 14.4 and realized on FPGA.

I. INTRODUCTION

The main challenging in the VLSI circuits are area cost power performance reliability and demand for portable computing devices is also increasing. These applications require low power dissipation circuits.

Different techniques are available to reduce the switching activities of test patterns. For linear feedback shift register (LFSR), a modified clock scheme in which only half of the D flip-flops works, thus only half of the test pattern can be switched. This can reduce the average power compared to traditional linear feedback shift register (LFSR).A better low power can be achieved by using single input change pattern generators. The combination of LFSR and scan shift register is used to generate random single input charge sequence, it is proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. In it is proposed that 2m single input changing data is inserted between two neighboring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

II. BIST TECHNIQUE

VLSI testing problems like Test generation problems,input combinatorial problems, gate to I/O pin ratio problems are discussed [3] and this motivated designers to identify reliable test methods in solving these difficulties. An insertion of special test circuitry on the VLSI circuit that allows efficient test coverage is the answer to the matter.This has been addressed by the need for design for testability (DFT) and hence the need for BIST. BIST is an on-chip test logic that is utilized to test the functional logic of a chip, by itself. Fig. 1shows a BIST module composition.

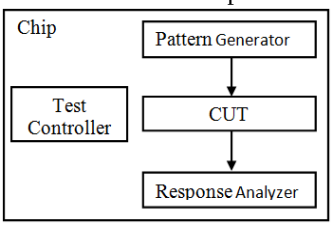


Fig 1:Generic BIST architecture

III. PROPOSED METHOD

In this paper, we proposed a novel architecture which generates the test patterns with reduced switching activities. LP-TPG structure consists of modified low power linear feedback shift register (LPLFSR), m-bit counter, gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated

from LP-LFSR is Exclusive–ORed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.

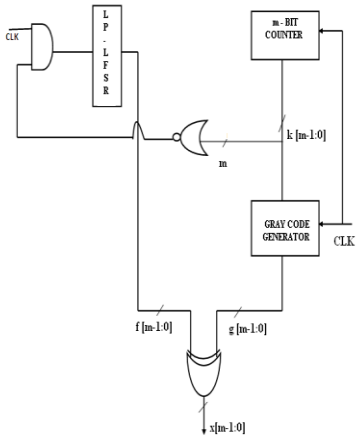


Figure 2. Low Power Test Pattern Generator

IV. ALGORITHM FOR LP-LFSR

The algorithm for LP-LFSR is given below: Consider a N-bit external (or) internal linear feedback shift register [n>2].

- For example n-bit, external LFSR is taken, which consists of n-flip flops in series. A common clock signal is applied as control signal for all flip flop.
- For exchanging the output of adjacent flip flops, multiplexers are used. The output of the last stage flip flop is taken as a select line.
- If the last stage flip flop output is one, any one of the flip flop output is swapped with its adjacent flip flop output value.
- If the last stage flip flop output is Zero, no swapping will be carried out.
- The output from other flip flops will be taken as such.
- If the LFSR is moved through a complete cycle of 2n states then the transitions expected are 2n-1.When the output of the adjacent flip flops are swapped, the expected transitions are 2n-2.Thus the transitions produced are reduced by 50% compared with original LFSR. The transition reduction is concentrated mainly on any one of the multiplexer output.
- Gray converter modifies the counter output such that two successive values of its output are differing in only one bit. Gray converters can be implemented as shown below.

g[n-1]= k [n-1]
g[n-2]= k [n-1] XOR k[n-2]
.
.
g[2]= k [2] XOR k[3]
3336
g[1]= k[1] XOR k[2]
g[0]= k[0] XOR k[1]

In [12] it is stated that that the conventional LFSR's outputs cannot be taken as the seed directly, because some seeds may share the same vectors. Thus the LP-LFSR should ensure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. Test patterns generated from the proposed structure are implemented as following equations.

x[0] = f[0] XOR g[0]
x[1] = f[1] XOR g[1]
x[2] = f[2] XOR g[2]
x[3] = f[3] XOR g[3]
x[4] = f[4] XOR g[4]
x[5] = f[5] XOR g[5]
.
..
X [n-1] = f[n-1] XOR g[n-1]

Thus the XOR result of the sequences is single input changing sequence. In turn reduces the switching activity and so power dissipation is very less compared with conventional LFSR. Fig. 2 is an example of counter and its respective gray value. It is shown that all values of g[2:0] are single input changing patterns.

Patterns**:**
K [2:0] g [2:0]
K0= 000 g0= 000
K1= 001 g1= 001
K2= 010 g2= 011
K3= 011 g3= 010
K4= 100 g4= 110
K5= 101 g5= 111
K6= 110 g6= 101
K7= 111 g7= 100

V. UART Transmitter

The transmitter accepts parallel data from peripheral/processor, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal (fig. 3). The baud rate generator output will be the clock for UART transmitter

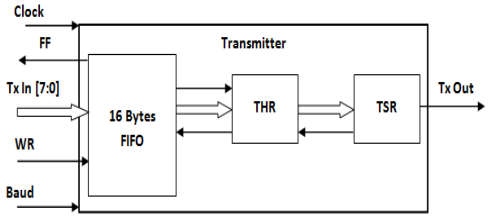


Fig. 3: UART Transmitter

VI. UART Receiver

The received serial data is available on the RXIN pin. The received data is applied to the sampling logic block. The receiver timing and control is used for synchronization of clock signal between transmitter and receiver. The receiver sampling is 16 times to that of the transmitter baud rate. In the architecture of

UART receiver (fig. 4), initially the logic line (RxIn) is high.

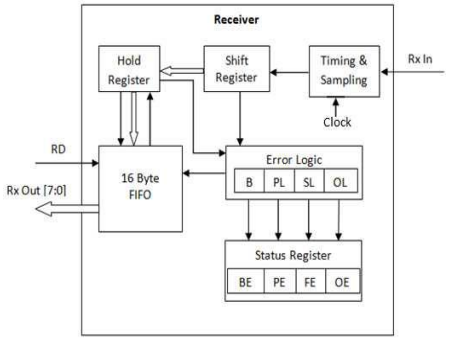


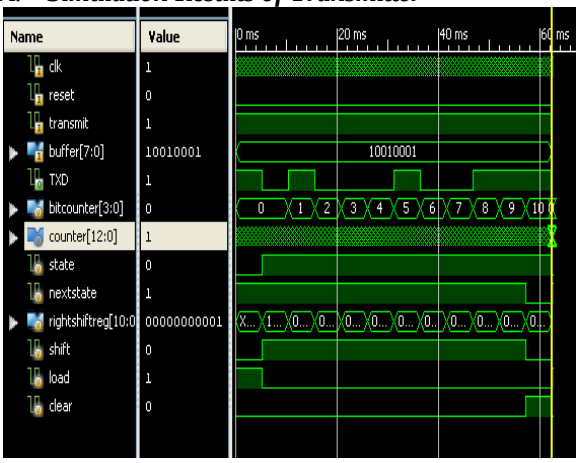
Fig. 4: UART Receiver

Whenever it goes low sampling and logic block will take 4 samples of that bit and if all four are same it indicates the start of a frame. After that remaining bits are sampled in the same way and all the bits are send to Receiver Shift Register (RSR) one by one where the entire frame is stored. RSR is a 12 bit shift register.

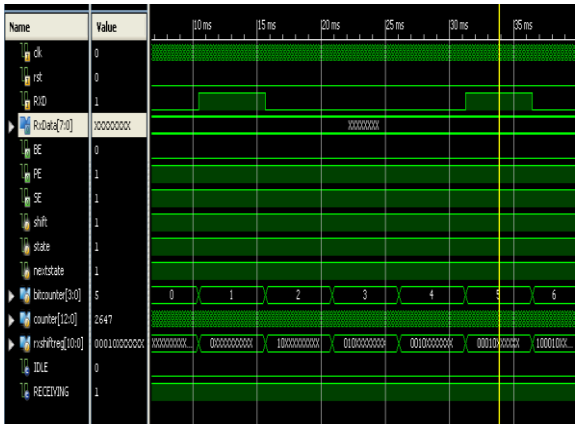
VII. SIMULATION RESULTS

The verilog HDL coding and simulation of the design are done in Xilinx tool ISim 14.4. The operating clock frequency used for simulation is 50 MHz. The baud rate set is 9600bps. Data word length is 8-bits.

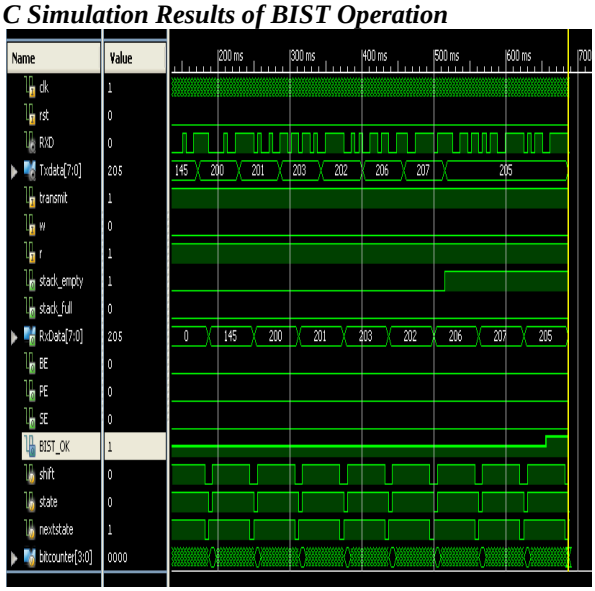
A. Simulation Results of Transmitter



B Simulation Results of Receiver



C Simulation Results of BIST Operation

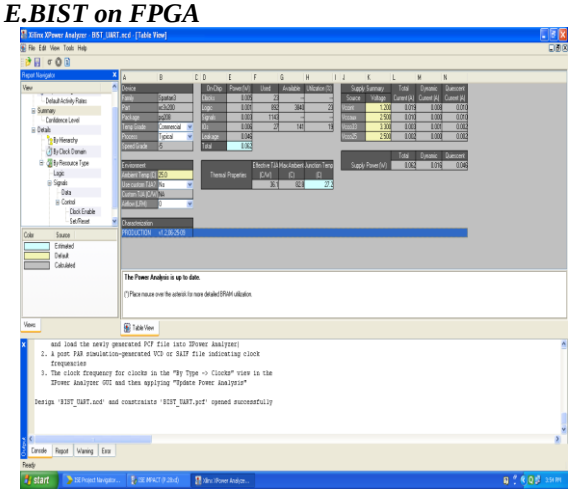


D. Synthesis Report

Table II Design implementation summary

Speed Grade	-4
Minimum period	13.204ns (Maximum Frequency: 75.733MHz)
Minimum input arrival time before clock	9.280ns
Maximum output required time after clock	6.083ns
Maximum combinational path delay	No path found

E.BIST on FPGA



VIII. CONCLUSION

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator.

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